IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chen, et al.	§	Attorney Docket No. 24061.42
	§	
	§	Customer No. 27683
Serial No. 10/712460	§	
	§	Group Art Unit: Unknown
Filed: November 13, 2003	§	
	§	Examiner: Unknown
For: SEMICONDUCTOR WAFER MANUFACTURING METHODS EMPLOYING CLEANING DELAY PERIOD	§	

LETTER TO THE OFFICIAL DRAFTSPERSON

Attn: Official Draftsperson
Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed are two (2) sheets of formal drawings to replace the informal drawings as originally filed in the above-identified patent application.

Respectfully submitted,

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Date: December 11, 2003
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File: 24061.42
R-62041

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on December 11, 2003.

Gayle Conner